

# Optimization of Stacked Passivation for Mid and Long Wavelength InAs/GaSb Superlattice Photodetectors

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**ABSTRACT-** *Stacked passivation is investigated to enhance the long term stability of the interface between the passivation layer and InAs/GaSb substrate for application in infrared photodiodes. ZnS/Silicon nitride, ZnS/Silicon oxide and ZnS passivation layers were intended to be compared on the basis of their capacitance-voltage characteristics and dynamic resistance measurements. Attempts at surface passivation using ZnS were unsuccessful because the samples displayed poor electrical insulation. We were unable to improve the long term performance of the devices by preventing the degradation of ZnS over time. Thus, the focus of this work shifted to the optimization of low-stress silicon nitride passivation layers. Our research indicates that we can alter the mechanical properties of SiN thin films by changing the gas flow rates during plasma-enhanced chemical vapor deposition (PECVD). We expect that the passivation quality and electrical properties of silicon nitride thin films are highly dependent upon the gas flow ratio.*

## I. INTRODUCTION

Indium arsenide/gallium antimonide (InAs/GaSb) type-II strained superlattice materials have been identified as an alternative to conventional mercury cadmium telluride (HgCdTe) detectors in the mid- and long –wavelength infrared (MWIR and LWIR) spectrum. Unlike other commonly used materials, InAs and GaSb have misaligned band structures which reduce the detrimental effects of recombination<sup>1</sup>. In addition, this superlattice material has ideal optical absorption properties and can be easily grown to meet the requirements of long wavelength infrared devices<sup>2</sup>. However, being a small bandgap material, its performance so far has been limited by poor surface quality; even a low density of surface defects can cause a significant deterioration in the device performance.

These infrared detectors have important applications in industry, military, space and medical disciplines where varying wavelength intensities allow for thermal imaging. Yet, due to poor surface stability, InAs/GaSb superlattice detectors are still unable to meet demands necessary for commercialization. Surface leakage, the major component of the total dark current, caused by interfacial traps, oxide charges and conductive oxides have limited the performance of these devices so far. The most significant contribution to surface leakage comes from interfacial traps, which form from the abrupt termination of the crystal structure at a surface. As a result of the termination, dangling or unsatisfied bonds create energy states in the otherwise forbidden area near the material's surface<sup>1</sup>. These traps create an unwanted surface current. In addition, native oxides that form during exposure to the atmosphere are often naturally conductive, therefore, providing a leakage path at the surface. Furthermore, charged ions incorporated in the oxide layer during processing can add to the problem through band bending near the surface<sup>4</sup>.

Surface passivation provides a viable solution to the problems associated with surface leakage. An optimum passivation layer over the exposed device surfaces will prevent current flow in the oxide and terminate the unsatisfied bonds in the semiconductor surface, thereby improving device performance. An earlier comparative study of silicon nitride (SiN), silicon dioxide (SiO<sub>2</sub>) and Zinc Sulfide (ZnS) passivants found that zinc sulfide out-performed the other

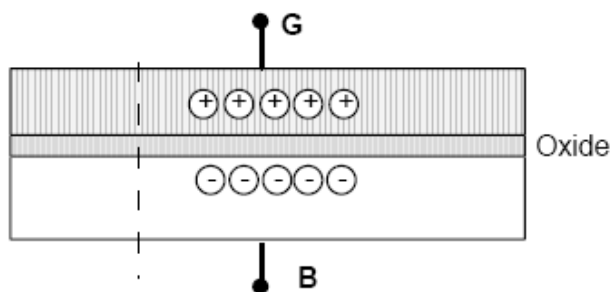
passivants followed by SiN and SiO<sub>2</sub> for InAs/GaSb photodetectors<sup>3</sup>. ZnS allows for a high quality semiconductor/passivant interface with minimum surface traps and oxide charges. Its refractive index and minimal thickness allow for maximum transmission of incoming photons, and its thermal expansion coefficient matches that of InAs/GaSb so there is no thermally generated strain during temperature fluctuations<sup>2</sup>. However, further investigation of the ZnS passivation layer found that it degrades over time. This degradation is caused by the absorption of water vapor from the atmosphere and electron bombardment from radiation<sup>5,6</sup>. In this study, stacked passivation is investigated to prevent ZnS degradation and improve the performance of these detectors over time. ZnS/silicon nitride and ZnS/silicon oxide were chosen to form the stacked passivation layers, and the electrical properties of the devices were explored with capacitance-voltage (C-V) characteristics and dynamic resistance measurements.

## II. THE IDEAL MIS DEVICE

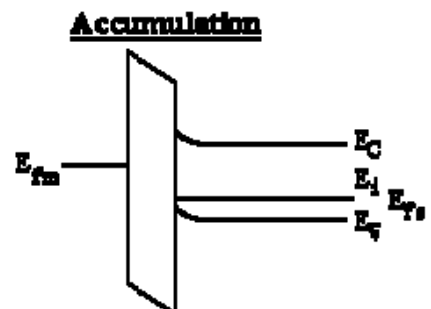
Analysis of the surface states in metal-insulator-semiconductor (MIS) structures is central to improving interface properties, thus leading to increased performance in InAs/GaSb devices. Because these devices are designed to detect the MWIR and LWIR spectrum, the bandgap in the semiconductor must be narrow to ensure that the energy of the incoming photon is sufficient to generate a photocurrent<sup>7</sup>. In narrow bandgap materials, a small amount of surface defects can significantly change the device characteristics<sup>2</sup>. Therefore, optimal surface conditions with trap-free and high resistive passivants are essential.

The MIS structure is essentially a capacitor in which one plate is a semiconductor. This geometry sets up an electric field over the insulating layer. In this study, the sandwich structure is composed of an InAs/GaSb superlattice semiconductor, a ZnS or stacked insulating layer and a gold metal contact or gate electrode. When a voltage is applied across the structure, it modifies the distribution of charges in the semiconductor giving rise to three distinct surface conditions: accumulation, depletion and inversion<sup>8</sup>.

For simplicity, we will use a metal-oxide-semiconductor (MOS) capacitor to describe these biasing regions. Taking the silicon substrate to be n-type, the application of a positive bias deposits positive charge on the metal. To maintain charge balance, an equal net negative charge is induced at the semiconductor surface by the accumulation of mobile electrons (Fig. 1). This situation, described by a large concentration of mobile carriers at the interface, is known as *accumulation*<sup>8</sup>. Internally, this charge modification results in band bending near the surface of

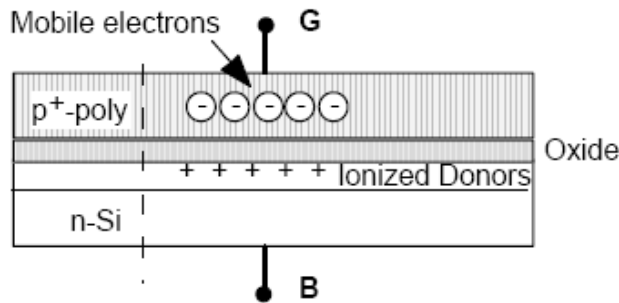


**Figure 1.** Charge distribution of a MOS capacitor in accumulation<sup>8</sup>.  
the semiconductor as pictured in Fig. 2.

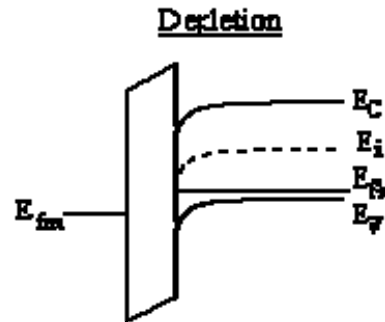


**Figure 2.** Energy band diagram corresponding to accumulation ( $V_G > 0$ )<sup>10</sup>.

Now we consider the application of a negative gate voltage. A negative charge applied to the metal repels mobile electrons from the oxide-semiconductor interface leaving behind fixed positive charges. This condition, in which the concentration of mobile carriers at the interface is less than in the bulk, is known as *depletion*<sup>8</sup> (Fig. 3). This charge modification induces band bending that is opposite to that of accumulation as seen in Fig. 4.

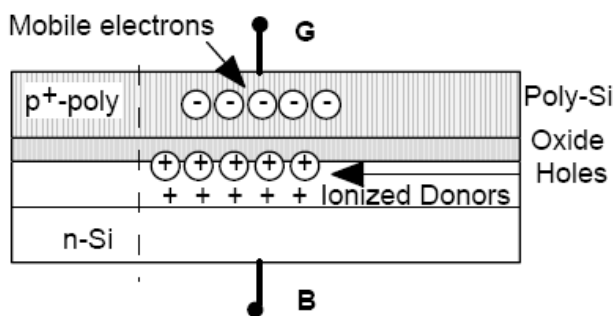


**Figure 3.** Charge Distribution of a MOS capacitor in depletion<sup>8</sup>.

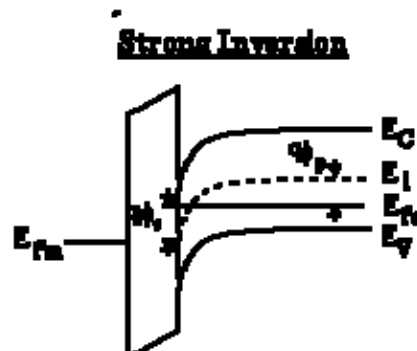


**Figure 4.** Energy band diagram corresponding to depletion ( $V_G < 0$ )<sup>10</sup>.

Finally, we consider the effects of an even higher negative bias. As the gate voltage becomes increasingly negative, the depletion region reaches a maximum. In order to maintain charge balance, holes gather at the semiconductor surface to accommodate for the increasingly negative gate voltage. At a particular threshold voltage, the surface is no longer depleted and, in fact, changes from n-type to p-type. “This situation where minority carrier concentration at the surface exceeds the bulk majority carrier concentration is referred to as *inversion*”<sup>8</sup>. The corresponding energy band diagram is shown in Figure 6.



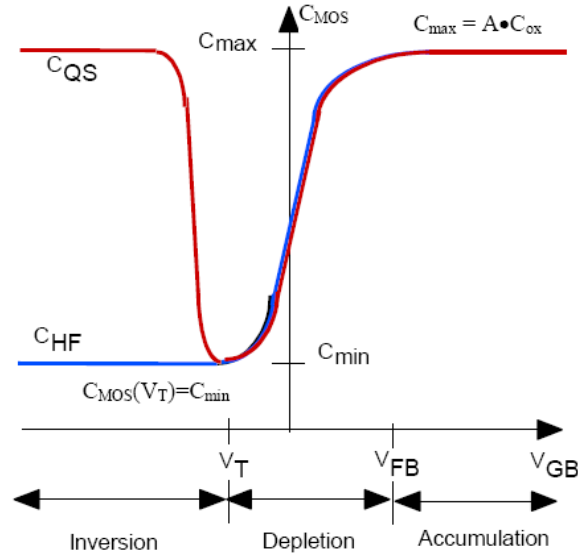
**Figure 5.** Charge distribution of a MOS capacitor biased into inversion<sup>8</sup>.



**Figure 6.** Energy band diagram corresponding to inversion ( $V_G < V_T$ )<sup>10</sup>.

The capacitance of these devices depends on the applied voltage. This dependence can be seen in the capacitance-voltage curve in Figure 7. The flatband voltage, which separates the accumulation and depletion regions, marks the spot where there is no charge on the plates of the capacitor and thus no band bending<sup>8</sup>. This ideally occurs at  $V_{FB} = 0$ . The flatband voltage is of particular interest in this study because it depends on the number of fixed interface charges. A flatband voltage above or below zero indicates that there is band bending caused by the presence of surface charges<sup>8</sup>. Based on the C-V curves we can determine the flatband voltage, and from

the flatband voltage, we can determine the effective oxide charge at the interface<sup>11</sup>. Since our goal is to reduce interface trap density and fixed oxide charges, this is an effective measurement of the quality of the surface passivation. Optimal operation of photodetectors requires flatband surface conditions<sup>9</sup>.



**Figure 7.** Capacitance vs. Gate Voltage in an MOS capacitor. Flatband voltage marks the dividing line between accumulation and depletion and the threshold voltage is marks the depletion-inversion transition.  $C_{HF}$  is high frequency and  $C_{QS}$  is low frequency.<sup>8</sup>

It is important to note that the difference in the two curves in the inversion region is a result of high frequency or low frequency measurements. At a high frequency signal ( $f=1\text{MHz}$ ), “the generation rate of electron-hole pairs is not fast enough to allow the formation of a hole charge density at the interface”<sup>8</sup>. Therefore, the depletion region remains at a maximum value and capacitance is at a minimum. At a low frequency signal, the generation rate is fast enough so that electron-hole pairs are swept aside by the electric field creating a thin layer of charge<sup>8</sup>.

### III. DEVICE FABRICATION

The MIS structure is created by depositing a  $4000\text{\AA}$  ZnS insulation layer on top of the InAs/GaSb semiconductor by electron-beam deposition at room temperature. The deposition rate is kept low initially ( $0.7\text{-}0.8\text{ \AA/s}$ ) and then increased to  $1\text{-}1.2\text{ \AA/s}$ . The rate and the total thickness is monitored in situ using a crystal in the deposition chamber. A  $300\text{\AA}$  SiN layer is subsequently deposited using plasma enhanced chemical vapor deposition. Finally, a  $1500\text{\AA}$  gold metal contact is deposited with electron-beam deposition to form the gate electrode. Capacitance-voltage (C-V) characteristics are measured to assess the quality of the semiconductor-passivant interface.

#### IV. EXPERIMENTAL RESULTS AND DISCUSSTION

Attempts at surface passivation using ZnS were unsuccessful because the samples displayed poor electrical insulation. Causes of the problem are not yet clear, however, the samples were outsourced to a third party so the deposition conditions of the film are still under investigation. Since we were unable to take electrical measurements, we could not examine the effectiveness of stacked passivation in preventing degradation of ZnS over time, and therefore, have no data on the long term performance of these devices. Instead we chose to shift our focus to the optimization of silicon nitride passivation, which was determined to be the second best passivant based on the results of earlier studies<sup>3</sup>.

Silicon nitride films offer many advantages as a passivation layer for InAs/GaSb detectors; they are a high quality dielectric, hard and strong and have high resistivity and low porosity, however, they possess a high mechanical stress<sup>12,13</sup>. This stress is composed of two components; intrinsic and thermal. The intrinsic stress comes about during deposition of the thin film as a result of the silicon nitride structure, while the thermal component is a result of different coefficients of expansion between the deposited layer and the substrate<sup>14</sup>. In microelectronics, this strain can be very detrimental to device performance as it is typically associated with surface defects<sup>15</sup>. Moreover, these microelectronic devices require processing temperatures below 400°C so silicon nitride films are produced by plasma-enhanced CVD “where process gases are excited in a radio frequency field between two parallel plate electrodes”<sup>12</sup>. However, there is an inverse relation between temperature and hydrogen content; as temperature decreases hydrogen increases. The incorporation of hydrogen disrupts Si-N bonds which also contribute to total stress<sup>13</sup>. In addition, hydrogen can diffuse from the nitrogen and generate traps at the interface<sup>12</sup>.

It has been confirmed by many studies that changing the processing conditions significantly alters the film composition and thus the mechanical properties<sup>13,14,15</sup>. The general consensus is that there is a linear increase in strain as the nitrogen content is increased<sup>14</sup>. While many studies have reported the effect of the plasma-enhanced CVD process on the mechanical properties of silicon nitride films, none of these studies have investigated the effects on electrical properties. We believe that electrical performance of these devices will be strongly dependent on the ratio of process gas flow (silane (SiH<sub>4</sub>) and ammonia (NH<sub>3</sub>)). It is likely that the excessive strain in devices passivated with silicon nitride films increases the surface leakage of these devices. By depositing silicon-rich films, we hope to reduce the factors limiting the passivation quality.

A preliminary SiN film was deposited by PECVD from silane (SiH<sub>4</sub>) and ammonia (NH<sub>3</sub>) on a dummy wafer for 15 minutes. The following deposition parameters were used: temperature 300°C, pressure 650mtorr, and gaseous flow rates for silane and ammonia were 500sccm and 70sccm, respectively. A film thickness of 265nm and a refractive index of 1.95 were determined by ellipsometry. Based on data presented by French and Sarro<sup>15</sup>, our results seem promising. The next step will be to fabricate actual photodetectors and observe the electrical properties of the devices as a result of changes in the gas-flow ratio during deposition. We expect that low stress (silicon-rich) silicon nitride films will improve device performance compared to stoichiometric Si<sub>3</sub>N<sub>4</sub> passivation layers. To date, we have been unable to test detectors due to time constraints and limited resources.

## **V. CONCLUSION**

We had hoped to monitor the performance of stacked passivation on InAs/GaSb devices using capacitance-voltage (C-V) characteristics and subsequently dark current/dynamic resistance measurements on fabricated photodetectors. However, we were unable to achieve good electrical insulation on these devices and, therefore, have no data on the long term stability of the interface between the passivation layer and InAs/GaSb substrate. Due to time constraints, we had to switch to the second choice passivant, SiN; however, that's not to rule out the possibilities of ZnS. Given more time, ZnS may indeed be the better choice.

We have just begun to lay the groundwork for optimizing SiN passivation. Research suggests that changing the Si/N ratio significantly alters the mechanical properties of the thin films. We suspect that changes in the mechanical properties of the films will also affect the electrical properties and passivation quality. We have conducted one preliminary test with good results. Next we will fabricate detectors to test the effects of changes in the gas-flow ratio during PECVD.

## **ACKNOWLEDGEMENT**

Special thanks to my advisor Professor Sid Ghosh and to Koushik Banerjee. This project was funded by the National Science Foundation and the Department of Defense from the EEC-NSF Grant # 0755115. Additional financial support was awarded by the National Science Foundation from the CMMI-NSF Grant # 0925425.

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